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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/548,942 | 04/13/2000 | Warren M. Farnworth | 4161US (98-1265) | 6934 |

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2817 | |

DATE MAILED: 01/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/548,942 | FARNWORTH, WARREN M. | |
| | Examiner | Art Unit | |
| | Benny Lee | 2817 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *25 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *24-26 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-26, 28-30; 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 25 October 2005 has been entered.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the solder balls being connected to at least one signal and at least connected to the voltage reference signal (e.g. cls 24, 31) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification needs to provide an explicit description with respect to the Fig. 11 embodiment of the connection of the solder balls to at least one signal trace and the voltage reference signal as recited in amended claims 24, 31. Since this amended limitation is considered not to be "new matter", then an amendment to the fig. 11 description adding the amended claim limitation would be appropriate..

Claims 24-26, 28-30; 31 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claims 24, 31, it is noted that these amended claims recites inter alia: a "semiconductor substrate" having a structure with a voltage reference plane "substantially covering" a surface of the substrate and including "signal trace slots" therein, where signal traces are "disposed in the slots" to provide electrical isolation between the signal traces, and further having solder balls connected to the signal traces and voltage reference signal. It appears that the reference to the "semiconductor substrate" and "solder balls" relates to the embodiment depicted and described relative to "figure 11", while the reference to the slotted voltage reference plane and isolated signal traces relate to the embodiment of "figure 13". However, there does not appear to be any

disclosure in the original specification as to an embodiment combining the "semiconductor substrate/solder balls' embodiment of "figure 11" with the slotted voltage reference plane/isolated signal traces embodiment of "figure 13". Therefore, it is unclear whether applicant actually "possessed" this combination embodiment at the time the application was filed. Accordingly, these claims have been treated as "new matter".

Regarding claims 28-30, it is noted that this claim, as amended, now requires the "semiconductor substrate" to include "an electrically insulative layer". However, there does not appear to be any disclosure in the original specification to provide for a combination of the "semiconductor substrate" being "an electrically insulating layer" as presently recited in these claims, and thus this limitation has been treated as "new matter".

However, if applicant does not believe the above cited issues are "new matter", then an appropriate explanation is required to be provided, including pointing out where in the original disclosure, explicit and/or implicit support for the subject matter of the above cited claims can be found.

Claims 28-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 28, 29, 30, note that it is unclear whether the recited "electrically insulative layer" can properly depend from or properly further limit a "substrate" which as been previously defined as being a "semiconductor". That is to say, a "semiconductor" has material properties which are materially different from that of "an electrically

insulative layer" and as such would appear incompatible with it's use as a "semiconductor substrate". Clarification is needed.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 24, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kakimoto et al ('278) in view of Caillat et al.

Kakimoto et al discloses in fig. 21 thereof, a ground and signal trace pattern configuration disposed on a surface of a semiconductor substrate (20). Note that the pattern comprises a voltage reference or ground plane (21) substantially surrounding the surface of the semiconductor substrate and patterned to include slots therein. The slots in the ground pattern are filled with signal trace portions, which are electrically isolated from each other by the intervening ground plane portions. Note that certain signal traces are configured to have a change in direction. Furthermore, note that both the ground plane and the signal traces have terminal connections (e.g. 37b, 37a), which provide respective connection to a circuit board (e.g. see Fig. 19). However, such connection terminals have not been disclosed as being a solder ball connection, as recited in claim 24.

Caillat et al discloses the use of conductive spheres (i.e. balls), which connect the semiconductor integrated circuit (e.g. 56) to conductors (e.g. 48, 50, 52) located on a substrate or printed circuit board.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have realized the connection means (37) of Kakimoto et al as solder balls or spheres as taught by Caillat et al. Such a modification would have been considered an

obvious substitution of art recognized equivalent means of connecting a semiconductor circuit to a circuit board, especially since Kakimoto et al recognizes the use of varied connection structures between the semiconductor structure and the circuit board (e.g. Figs. 19, 20D, etc), thereby suggesting the obviousness of such a modification.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lampen et al in view of Caillat et al.

Lampen et al in fig. 6 discloses a semiconductive MMIC having a ground or voltage reference plane (68) disposed over substantially the entire surface of the MMIC. Moreover, note that the ground plane includes a plurality of slots (72) disposed therein in which respective short conductive traces or pads (70) are disposed. Furthermore, note that the traces are disposed such that the ground plane electrically isolates adjacent conductive traces. As evident from Fig. 7, the MMIC can be mounted to a substrate (26) of a circuit board through a plurality of connection means (52, 52A, 52B), which electrically connect the ground plane and conductive traces, respectively to corresponding conductive layers on the substrate. However, Lampen et al differs from the claimed invention in that the connection means are not explicitly disclosed as solder balls.

However, as taught by Caillat et al, the use of conductive spheres or balls for connecting a semiconductive IC to a circuit board is recognized as conventional in the art.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have realized the connection means (52, 52A, 52B) of Lampen et al as solder balls or spheres as taught by Caillat et al. Such a modification would have been considered an obvious substitution of art recognized equivalent means of connecting a

semiconductor circuit to a circuit board, thereby suggesting the obviousness of such a modification.

Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over either of the preceding rejections as applied to claim24 above, and further in view of Quan (of record).

As described in either of the preceding rejections, the obvious combination of references meets the claimed invention except for the presence of a passivation layer, as claimed herein.

As described in previous Office actions Quan discloses that the use of passivation layers to isolate conductors on a substrate is well known in the art.

Accordingly, it would have been obvious in view of the references, taken as a whole, to have further modified either of the above combinations to have included a passivation layer, such as taught by Quan. Such a modification would have provided the advantageous benefit of providing further electrical isolation of the electrical signal traces in the combination, thereby suggesting the obviousness of such a modification.

Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Forbes et al (of record) in view of either Kakimoto et al or Lampen et al as modified by Caillat et al.

As described in previous Office actions, Forbes discloses an electronic system including a processor, memory device, input device, output device, data storage device, etc, but does not disclose such devices being semiconductor substrates having the recited conductive patterns connected by solder balls. As described in the preceding rejections,

the formation of a semiconductor substrate having the recited conductive patterns and connected by solder balls was considered obvious for reason stated in these rejections.

Accordingly, it would have been obvious to have realized any one of the circuit components in Forbes et al by either the Kakimoto et al or Lampen et al semiconductor substrate as modified by Caillat et al to have included solder balls. Such a modification would have been considered an obvious substitution of art recognized semiconductor structures, especially in view of the compatability of the semiconductor components in Forbes to the semiconductor structure in either combination, thereby suggesting the obviousness of such a modification.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kakimoto et al ('660) discloses the mounting of a semiconductor substrate having isolated signal traces to a circuit board.

Any inquiry concerning this communication should be directed to Benny Lee at telephone number 571 272 1764.

B. Lee

Benny Lee

BENNY T. LEE
PRIMARY EXAMINER
ART UNIT 2817